Cmt A6

The drain current of device M2 is shown as waveform 620, and is graphed as a function of time along X axis 624.

Please replace the paragraph starting on page 13 line 10 and ending on page 13 line 18 with the following paragraph:

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The amplitude of the IF signal provided by the downconverter is detected by RSSI block 940 and presented to the baseband circuit 945. The RSSI block 940 may receive an input from one or both of the outputs of the low pass filters 930 and 932. Alternately, or in combination, the RSSI block may receive an input from one or both of the outputs of the mixers 920 and 925. RSSI block 940 may contain logarithmic amplifiers and rectifiers. Examples of such logarithmic amplifiers can be found in jointly assigned, copending U.S. application number 09/836,624, filed April 16, 2001, attorney docket number 20408-001300US, titled "Logarithmic IF Amplifier with Dynamic Large Signal Bias Current, which is hereby incorporated by reference.

IN THE CLAIMS:

Please amend claim 1 as indicated. Please cancel claims 7-15 without prejudice. Please add new claims 22-30.

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1. (Amended) A method of buffering an input signal comprising:

receiving the input signal, wherein the input signal alternates between a first polarity and a second polarity;

generating a first current, wherein the first current is proportional to the input signal when the input signal has the first polarity, and approximately equal to zero when the input signal has the second polarity;

generating a second current, wherein the second current is proportional to the input signal when the input signal has the second polarity, and approximately equal to zero when the input signal has the first polarity;

generating a third current proportional to the first current;

generating a fourth current proportional to the second current;
applying the first and fourth currents to a first terminal of an inductor; and
applying the second and third currents to a second terminal of the inductor.

22. (New) A method of buffering an RF signal comprising:
receiving the RF signal, wherein the RF signal alternates between a first polarity and a second polarity;
generating a first current, wherein the first current is proportional to the RF signal when the RF signal has the first polarity, and approximately equal to zero when the RF signal has the second polarity;
generating a second current, wherein the second current is proportional to the RF signal when the RF signal has the second polarity, and approximately equal to zero when the RF signal has the first polarity;
using the first current to generate a third current, the third current proportional to the first current;
using the second current to generate a fourth current, the fourth current proportional to the second current;
applying the first and fourth currents to a first terminal of an inductor; and
applying the second and third currents to a second terminal of the inductor.

23. (New) The method of claim 22 wherein a capacitance is coupled between the first terminal of the inductor and the second terminal of the inductor, and the inductor and capacitance form a tank circuit.

24. (New) The method of claim 23 wherein the input signal alternates between the first polarity and the second polarity at a first frequency, the tank circuit has a resonant frequency of a second frequency, and the first frequency and second frequency are approximately equal.

25. (New) The method of claim 22 wherein the first current is geometrically proportional to the input signal when the input signal has the first polarity, and the second current is geometrically proportional to the input signal when the input signal has the second polarity.

26. (New) An RF amplifier comprising:

a first device coupled between a first output node and a first supply node, having a control electrode configured to receive an RF signal, and further configured to operate near cutoff in the absence of the RF signal;

a second device coupled between a second output node and the first supply node, having a control electrode configured to receive a complement of the RF signal, and further configured to operate near cutoff in the absence of the complement of the RF signal;

a third device coupled between a second supply node and the first output node, having a control electrode coupled to the second output node;

a fourth device coupled between the second supply node and the second output node, having a control electrode coupled to the first output node; and

an inductor coupled between the first output node and the second output node.

27. (New) The circuit of claim 26 further comprising:

a fifth device coupled between the first device and the first output node; and

a sixth device coupled between the second device and the second output node.

28. (New) The circuit of claim 26 wherein the first device and the second device are NMOS devices, and the third device and fourth device are PMOS devices.

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29. (New) An integrated circuit, wherein the integrated circuit comprises the circuit of claim 28.

30. (New) A transceiver comprising the circuit of claim 28.

IN THE DRAWINGS:

Redlined and corrected versions of drawings 1, 2, 3, 8, and 10 are submitted for the Examiner's approval.